What is claimed is:

Sub A1>

1. A method of measuring the phase or frequency of a periodic input signal using a periodic reference signal, comprising:

comparing the input signal to the reference signal to obtain a lead signal and a lag signal; and

changing the count of an up/down counter in dependence on the input signal, the reference signal, the lead signal and the lag signal; and

using the lead signal, the lag signal and the count signal to produce a phase or frequency signal.

2. The method of Claim 1, wherein producing a phase or frequency signal comprises using the lead signal and the lag signal to form a difference signal, and filtering the difference signal to produce an aliased output signal.

3. The method of Claim 2, wherein producing a phase or frequency signal further comprises:

adding to the aliased output signal a correction signal representing a positive or negative phase increment to form an unwrapped output signal.

4. The method of Claim 3, wherein the correction signal is formed using the count of the up/down counter.

Sub A2>

5. Apparatus for measuring the phase or frequency of a periodic input signal using a periodic reference signal, comprising:

a comparison circuit for comparing the input signal to the reference signal to obtain a lead signal and a lag signal;

a logic circuit, including an up/down counter, responsive to the input signal, the reference signal, the lead signal and the lag signal to change the count of the up/down counter; and

means for using the lead signal, the lag signal and the count signal to produce a phase or frequency signal.

6. The apparatus of Claim 5, further comprising a pulse combiner/filter responsive to the lead signal and the lag signal to form a difference signal, and a filter for filtering the difference signal to produce an aliased output signal.

7. The apparatus of Claim 6, further comprising an adder for adding to the aliased output signal a correction signal representing a positive or negative phase increment to form an unwrapped output signal.

A2 Cont

8. The apparatus of Claim 7, further comprising circuitry for forming the correction signal using the count of the up/down counter.

9. The apparatus of Claim 8, wherein the circuitry for forming the correction signal comprises a multiplier having as one input signal a constant value and having as another input signal the count of the up/down counter.